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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/023,172	02/13/1998	THOMAS J. HOLMAN	042390.P5659	6584

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EXAMINER	
VERBRUGGE, KEVIN	
ART UNIT	**PAPER NUMBER**
2188	30

DATE MAILED: 05/05/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/023,172	HOLMAN, THOMAS J.	
	Examiner	Art Unit	
	Kevin Verbrugge	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 3/30/04 has been entered.

Response to Amendment

This final Office action is in response to Amendment E, paper #28, and the terminal disclaimer, paper #29, both filed 3/30/04 by fax with the RCE mentioned above. The amendment amended claim 15. Claims 15-31 are pending. All objections and rejections not repeated below are withdrawn.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 15-18, 20, 21, 26, and 28-30 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 4,045,781 to Levy et al., hereinafter simply Levy.

Regarding claim 15, Levy discloses memory modules with selectable byte addressing for a digital data processing system.

Levy shows the claimed first interface circuitry as the address (A), control (C), and data (D) lines in memory module 30 of Fig. 1 and portions of memory transceiver 41 and memory control and timing unit 42. These A, C, and D lines receive a memory request signal from a system memory controller (memory management unit 22 and associative memory 24) over a system memory bus (memory bus 40) as claimed. One portion of memory control and timing unit 42 that receives a memory request signal is the block labeled memory bus receivers 130A in Fig. 11.

He shows the claimed second interface circuitry as the low bus (data), high bus (data), and control and timing signal buses connected to memory transceiver 41 and memory control and timing unit 42. These lines couple a plurality of memory devices of the memory module as claimed.

He shows the claimed control logic as portions of memory transceiver 41 and memory control and timing circuit 42. Control signal generator 145 inside memory control and timing circuit 42, for example, shown in Fig. 11, generates signals for the memory devices as claimed.

Levy shows the claimed plurality of memory devices as low stacks 44 and high stacks 45.

Levy's first and second interfaces and control logic operate as claimed, serving as a direct interface between the plurality of memory devices and the system memory bus and system memory controller such that the plurality of memory devices and the system memory bus operate in different operating environments. Furthermore, the first and second interfaces and the control logic separate the plurality of memory devices from the system memory controller and the system memory bus as newly claimed.

Regarding claim 16, Levy's memory control and timing circuit 42 includes the claimed clock generator since it generates a clock signal to drive the separate signals controlling the plurality of memory devices as claimed. Fig. 11 shows memory control and timing circuit 42 in detail, including control signal generator 145 (which outputs CLK MDR BYTE 0-3 signals), read timing generator 152, and write timing generator 156.

Regarding claim 17, Levy's memory module controller includes the claimed request handling logic in memory transceiver 41 and memory control and timing unit 42 since it examines a memory request to determine whether the memory request is addressed to the memory devices in its module and ignores the request if it is not addressed to its memory devices as claimed. More specifically, Fig. 11 shows memory control and timing unit 42 in more detail and Fig. 20 shows memory transceiver 41 in more detail. Fig. 11 includes the claimed request handling logic as the address normalizing circuit 131A. If the memory is addressed to at least one of the memory devices on the module, then address normalizing circuit 131A permits the module to

process the request. Otherwise, if the address request is not addressed to one of the memory devices on the module, then address normalizing circuit 131A prevents further processing by the module by asserting the address out of range signal shown being input to start memory cycle logic 150 (see column 16, lines 1-23).

Regarding claim 18, Levy's memory module controller comprises the claimed power management unit because it controls power supplied to the memory devices as claimed. Levy's memory transceiver 41 and memory control and timing circuit 42 control all the signals and data supplied to the memory devices and thereby control the power supplied to the memory devices since power is transmitted on signals. In other words, power in the form of data, control, and timing signals is supplied to the memory devices. The broad language of the claim requires nothing more.

Regarding claim 20, since Levy's memory module controller does not send signals to its memory devices when a memory request is not addressed to any of the devices, it can be said that the memory controller reduces the power to the memory devices (since power is transmitted on the signals, as discussed in the rejection of claim 18 above).

Regarding claim 21, since Levy's memory module controller does not send signals to its memory devices when a memory request is not addressed to any of the

devices, it can be said that the memory controller decouples the memory devices from the memory bus.

Regarding claim 26, Levy's memory devices are volatile.

Regarding claim 28, Levy shows data handling logic as the circuitry of the memory transceiver 41 in Fig. 20.

Regarding claim 29, Levy shows the claimed writing buffer as latch 250 in Fig. 20, disclosed at column 22, lines 57 and following.

Regarding claim 30, Levy shows the claimed address storage unit as memory bus receivers 130A and memory address latch 154 in Fig. 11.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 19, 22-25, 27, and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al.

Regarding claim 19, Levy does not teach that his memory devices and the memory bus operate at different voltages. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levy's device to have the memory devices and the memory bus operate at different voltages to save power. It was well-known in the art at the time of the invention that operating devices at lower voltages reduces the total amount of power consumed, therefore the skilled artisan who was interested in saving the most power would have been motivated to design each component of the system to operate at the lowest possible voltage, thereby motivating him to modify Levy's device so the memory bus and the memory devices operated at different voltages.

Regarding claim 22, Levy does not teach altering the frequency of a clock signal to the memory devices when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claim 23, Levy does not teach disabling his clock generator when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claims 24 and 25, Levy does not disclose that his memory modules are SIMMs or DIMMs, perhaps because such terms were not used in the art at the time of his disclosure. However, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement his memory modules as SIMMs and DIMMs since those types of memory modules were common at the time of the invention.

Regarding claim 27, Levy does not explicitly mention any handshaking logic per se, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed handshaking logic to improve communications between the memory module controller and the system memory controller.

Regarding claim 31, Levy does not explicitly show the claimed read buffer, however, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include such a buffer so that data received from the memory devices could be held temporarily near the output of the memory module in case the memory bus were not available.

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Claims 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al. in view of U.S. Patent 5,257,233 to Schaefer.

Regarding claims 18, 20, and 21, Levy does not explicitly teach that his memory module controller comprises a power management unit.

Schaefer discloses a low power memory module using restricted RAM activation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Schaefer's power reduction circuitry and techniques in Levy's memory modules to reduce the amount of power consumed. Schaefer teaches that unused memory devices may be powered down or placed in a reduced power mode to reduce the amount of power consumed by the module as a whole. By powering down certain memory devices, they are effectively decoupled from the memory bus.

Regarding claim 19, neither Levy nor Schaefer teach that their memory devices and the memory bus operate at different voltages. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levy's device to have the memory devices and the memory bus operate at different voltages to save power. It was well-known in the art at the time of the invention that operating devices at lower voltages reduces the total amount of power consumed, therefore the skilled artisan who was interested in saving the most power would have been motivated to design each component of the system to operate at the lowest possible voltage, thereby

motivating him to modify Levy's device so the memory bus and the memory devices operated at different voltages.

Regarding claim 22, Levy does not teach altering the frequency of a clock signal to the memory devices when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claim 23, Levy does not teach disabling his clock generator when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

****

Claims 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 4,045,781 to Levy et al. in view of U.S. Patent 5,036,493 to Nielsen.

Regarding claims 18, 20, and 21, Levy does not explicitly teach that his memory module controller comprises a power management unit.

Nielsen discloses a system and method for reducing power usage by multiple memory modules.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to include Nielsen's power reduction circuitry and techniques in Levy's memory modules to reduce the amount of power consumed. Nielsen teaches that unused memory devices may be powered down or placed in a reduced power mode to reduce the amount of power consumed by the module as a whole. By powering down certain memory devices, they are effectively decoupled from the memory bus.

Regarding claim 19, neither Levy nor Nielsen teach that their memory devices and the memory bus operate at different voltages. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Levy's device to have the memory devices and the memory bus operate at different voltages to save power. It was well-known in the art at the time of the invention that operating devices at lower voltages reduces the total amount of power consumed, therefore the skilled artisan who was interested in saving the most power would have been motivated to design each component of the system to operate at the lowest possible voltage, thereby motivating him to modify Levy's device so the memory bus and the memory devices operated at different voltages.

Regarding claim 22, Levy does not teach altering the frequency of a clock signal to the memory devices when a memory request is not addressed to any of the memory

devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Regarding claim 23, Levy does not teach disabling his clock generator when a memory request is not addressed to any of the memory devices on a particular module, however it would have been obvious to one of ordinary skill in the art at the time the invention was made to do just that in order to save power.

Response to Arguments

On page 6 of the amendment, fourth paragraph, Applicant argues that "Claim 15 as [sic] presently amended to more clearly claim that the memory module controller serves as a direct interface to the system memory controller." However, the claim actually reads "the first and second interfaces and the control logic serve as a direct interface between the plurality of the memory devices and the system memory controller and the system memory bus."

Clearly Levy's first and second interfaces and the control logic serve as a direct interface between the plurality of memory devices (low stack units 44 and high stack units 45) and his system memory bus (memory bus 40). What is additionally asserted in this final Office action is that Levy's first and second interfaces and the control logic serve as a direct interface between the plurality of memory devices and his system memory controller (memory management unit 22 and associative memory 24), therefore the rejection is maintained and made final.

This modified characterization of Levy's system memory controller as including memory management unit 22 and associative memory 24 is entirely appropriate because of the extensive memory control functions performed by associative memory 24 as taught at column 7, lines 9-10 and line 34 through column 8, line 45, as well as columns 11-13. Additionally, some of the structure of associative memory 24 is shown in Fig. 8.

At page 7, first paragraph, first sentence, Applicant asserts "that Levy does not teach interfacing a system memory controller to a memory management unit." The Examiner had never asserted such, rather the Examiner is characterizing Levy's memory management unit (and now the associative memory) as his system memory controller. Perhaps Applicant meant that Levy does not teach interfacing a system memory controller to a memory module controller, but this is contradicted by the rest of Applicant's sentence where he asserts that Levy "teaches using an intermediate associative memory to interface a memory management unit to the memory control and timing/memory transceiver combination," which means that Levy's memory management unit does interface to his memory control and timing/memory transceiver combination (memory module controller), albeit indirectly, using an associative memory.

What is apparently being argued by Applicant is that Levy's system memory controller does not interface directly to his memory module controller but rather indirectly interfaces to his memory module controller, through his associative memory. However, the Examiner is now including Levy's associative memory as part of Levy's system memory controller since the associative memory performs some system

memory functions as mentioned above. This characterization of Levy's memory management unit 22 and his associative memory 24 together anticipating the claimed system memory controller is entirely appropriate since nothing in the claims precludes such an interpretation. Both the memory management unit 22 and the associative memory 24 reside in the processor system 20 and both perform system memory control functions, therefore it is appropriate to consider them as together anticipating the claimed system memory controller. As such, Levy's first and second interfaces and control logic serve as a direct interface between the plurality of memory devices and the system memory controller and the system memory bus as claimed.

Conclusion

All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

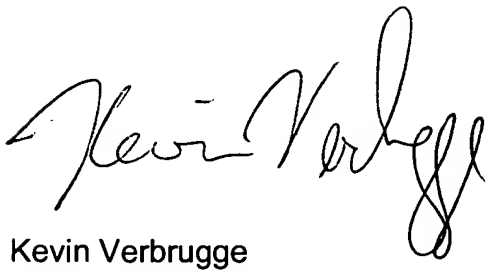
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the

shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning a communication from the Examiner should be directed to the Examiner by phone at (703) 308-6663.

Any response to this action should be labeled appropriately (serial number, Art Unit 2188, and After-Final, Official, or Draft) and mailed to Commissioner for Patents, Washington, D.C. 20231, faxed to (703) 872-9306, or delivered to Crystal Park 2, 2121 Crystal Drive, Arlington, VA, 4th Floor Receptionist.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197.



Kevin Verbrugge
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4/30/04